**SUBJECT-MECHATRONICS-I QUESTION BANK**

**CLASS-THIRD YEAR AT/WT**

**Q.1.MCQ**

Q1. The universal gate is ………………

1. NAND gate

2. OR gate

3. AND gate

4. None of the above

Q2. The inverter is ……………

1. NOT gate

2. OR gate

3. AND gate

4. None of the above

Q3. The inputs of a NAND gate are connected together. The resulting circuit is ………….

1. OR gate

2. AND gate

3. NOT gate

4. None of the above

Q4. The NOR gate is OR gate followed by ………………

1. AND gate

2. NAND gate

3. NOT gate

4. None of the above

Q5. The NAND gate is AND gate followed by …………………

1. NOT gate

2. OR gate

3. AND gate

4. None of the above

Q6. Digital circuit can be made by the repeated use of ………………

1. OR gates

2. NOT gates

3. NAND gates

4. None of the above

Q7. The only function of NOT gate is to ……………..

1. Stop signal

2. Invert input signal

3. Act as a universal gate

4. None of the above

Q8. In delay flip-flop, \_\_\_\_\_\_\_ after the propagation delay.

1. Input follows input

2. Input follows output

3. Output follows input

4. Output follows output

Q9. When both inputs of a J-K flip-flop cycle, the output will \_\_\_\_\_\_\_\_\_\_\_

1. Be invalid

2. Change

3. Not change

4. Toggle

Q10. How many types of sequential circuits are?

1. 2

2. 3

3. 4

4. 5

11. The basic latch consists of \_\_\_\_\_\_\_\_\_\_\_

1. Two inverters

2. Two comparators

3. Two amplifiers

4. Two adders

Q12. A counter is fundamentally a \_\_\_\_\_\_\_\_\_ sequential circuit that proceeds through the predetermined sequence of states only when input pulses are applied to it.

1. Register

2. Memory unit

3. flip-flop

4. arithmetic logic unit

Q13.BCD counter is also known as \_\_\_\_\_\_\_\_\_\_\_\_

1. Parallel counter

2. Decade counter

3. Synchronous counter

4. VLSI counter

Q14. A counter circuit is usually constructed of \_\_\_\_\_\_\_\_\_\_\_\_

1. A number of latches connected in cascade form

2. A number of NAND gates connected in cascade form

3. A number of flip-flops connected in cascade

4. A number of NOR gates connected in cascade form

Q 15. 555 timer pin 1 has

1. Ground

2. trigger

3. output

4. reset

Q16. A differential amplifier ……………..

1. Is a part of an Op-amp

2. Has one input and one output

3. Has two outputs

4. Answers (1) and (2)

Q17. For an Op-amp with negative feedback, the output is …….

1. Equal to the input

2. Increased

3. Fed back to the inverting input

4. Fed back to the noninverting input

Q18. The use of negative feedback ………

1. reduces the voltage gain of an Op-amp

2. Makes the Op-amp oscillate

3. Makes linear operation possible

4. Answers (1) and (2)

Q19. Negative feedback ………..

1. Increases the input and output impedances

2. increases the input impedance and bandwidth

3. Decreases the output impedance and bandwidth

4. Does not affect impedance or bandwidth

Q20.The Op-amp can amplify

1. a.c. signals only

2. d.c. signals only

3. both a.c. and d.c. signals

4. neither d.c. nor a.c. signals

**Q.2.EXPLAIN IN DETAIL 10 Marks**

1. Explain In Detail Logic Gates.

2. Explain In Detail Number System.

3. Explain In Detail binary Arithmetic

4. Explain In Detail Flip Flop.

5. Explain In Detail Op-Amp And What The Difference Between Linear And Non Linear Opamp Is.

6. Explain In Detail Timer Circuit.

7. Explain In Detail A to D Converter And D to A Converter.

8. What Is Flip Flop? Explain It’s All types In Detail

9. Explain In Detail Ripple Counter.

10. Explain In Detail Shift Register.

11. Explain In Detail Arithmetic Circuit.

**Q.3.Explain In Short 5Marks**

1. Explain Binary Codes

2. Explain Half Adder And Full Adder

3. Explain In Boolean Algebra

4. Explain S-R Flip Flop

5. Explain In Detail Op-Amp Parameters

6. Explain In Detail Ato D Converter

7. Explain In Detail Dto A Converter

8. Explain In Detail 555 Timer

9. Explain In Schmitt Trigger

10. Explain Linear Applications Of Op-Amps.

**Q4 WRITE A SHORT NOTE ON 5 Marks**

1. Logic Gates

2. Boolean Algebra

3. D/A Converter

4. A/D Converter

5. J-K Flip Flop

6. Arithmetic Circuit

7. Timer Circuit

8.555 Timer

9. Counter

10 Register

12. Op-Amp

13. Derived Gates